Proposal to Design Integrated Sensors

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Investigators: Jessica Metcalfe, Manoj Jadhav, Paul Reimer, Taylor Shin (Argonne National Laboratory)

Abstract: In the context of the TOPSiDE detector concept, we propose to design silicon sensors with integrated front-end readout. The sensors are based on the Low-Gain Avalanche Diode (LGAD) technology and feature ultra-fast signals, as required for a particle identifying, imaging calorimeter.

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Introduction: TOPSiDE

TOPSiDE [1] is a modern EIC detector concept based on novel detector paradigms and technologies recently developed by the High-Energy and Nuclear physics community. The tracking of charged particles is achieved with a precision vertex detector and a five-layer silicon tracker in the barrel region, supplemented with forward disks. The calorimeter is imaging, i.e. it features extremely fine granularity, both laterally and longitudinally. The particle identification (pion-kaon-proton separation) is achieved through precision timing in the calorimeter. In the very forward (hadron) region, the detector features a Ring Imaging Čerenkov counter (RICH), a dipole magnet, and additional tracking disks and again imaging calorimetry. In the backward (electron) direction, the necessary energy resolution is obtained by a crystal calorimeter, also with fine granularity. The central solenoid with a field of three Tesla is placed outside the calorimeter.

Advantages to this approach are many: Each particle produced in ep/eA collisions is measured individually with the subdetector providing the best momentum/energy resolution (Particle Flow paradigm) [3]; the energy resolution for neutral particles can be improved through software compensation techniques [4]; due to the imaging capability of the calorimeter, a muon identification system becomes redundant; the material in front of the calorimeter is minimized, as there is no need for additional time-of-flight counters, Čerenkov counters or Transition Radiation Detectors; the output of the detector is a list of identified particles with their momenta, similar to the hadron level output of Monte Carlo simulations.

The advantages for physics are many as well: higher photon detection efficiency (due to the minimal amount of 'dead' material in front of the calorimeter and hence an improved material budget); improved kinematic reconstruction, jet reconstruction, and background rejection (due to the excellent reconstruction (energy and angle) of the hadronic system), etc. This will result in an optimal use of the luminosity and provide precision measurements for all physics processes of interest at the EIC.

Introduction: Ultra-fast Silicon Detectors

The TOPSiDE concept requires Ultra-fast Silicon Detectors (UFSDs) with excellent timing resolution. GEANT4-based Monte Carlo simulations of TOPSiDE showed that a resolution of 10 picosecond or better is required to distinguish pions and kaons up to 7 GeV/c (the range of momenta for most of the solid angle).

UFSDs are being developed by various groups worldwide [5]. Currently, the best performance achieved a time resolution of 18 picosecond [6]. This was obtained with 35 μm thick sensors based on the Low-gain Avalanche Diode (LGAD) technology and read out by an external digitization system.

To further improve on these results, we propose to incorporate the readout system (digitization) into each pixel of the sensor. Apart from the expected improvement in time resolution, this will result in a significant cost savings for the final production.

Research program

In the following we detail the UFSD research program at Argonne. This is an ambitious and long-term endeavor including a number of subtasks which can be in part executed in parallel. Several items are already completed or already ongoing. This proposal applies mainly to items f and g:

a) Testing of silicon sensors

We acquired the necessary tools for testing UFSDs on the bench (GigaHertz oscilloscope, DC power supplies, signal processing computer, environmental chamber, and mechanical stands). We performed measurements of the IV and CV curves on several UFSDs obtained from collaborators at Torino, Santa Cruz, and BNL. We tested pairs of sensors in the Fermilab test beam to establish their time resolution. As an example, Fig. 1 shows the waveforms obtained from an HPK sensor in the primary 120 GeV proton beam. This is an ongoing effort with many more test beam campaigns expected in the future.

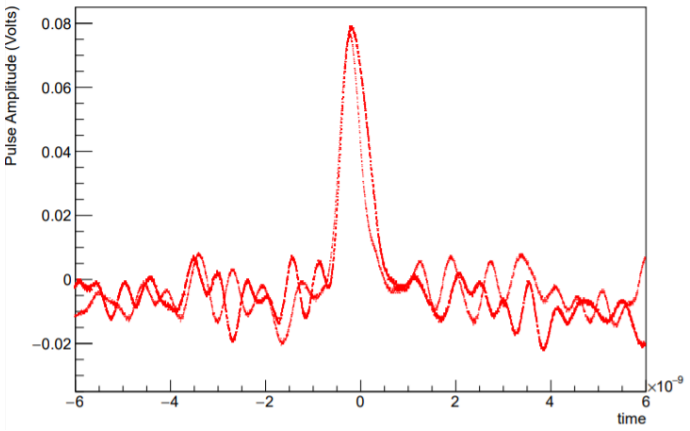

Figure 1. Waveforms recorded with an HPK sensor in the Fermilab test beam.

b) Development of a readout scheme

We developed a readout scheme for UFSDs (see Fig. 2), to be eventually implemented into each pixel. The signal from a given pixel is being shaped, amplified and its time-of-arrival as well as its time-over-threshold is being measured. To obtain the best possible time measurement a constant fraction discriminator is utilized, based on work performed by University of California Santa Cruz.

c) Design/simulation of an LGAD sensor

We completed the design/simulation of an LGAD sensor in terms of the physics of the silicon device, see Fig. 4. The sensor features the mandatory amplification layer responsible for the excellent timing characteristics with 1 x 1 mm^2 pads. Studies of the doping concentration, guard rings, temperature dependence etc. were performed with a commercial EDA tools called Silvaco ATLAS. As an example, we show in Fig. 3 the leakage current as function of doping concentration for different operating temperatures.

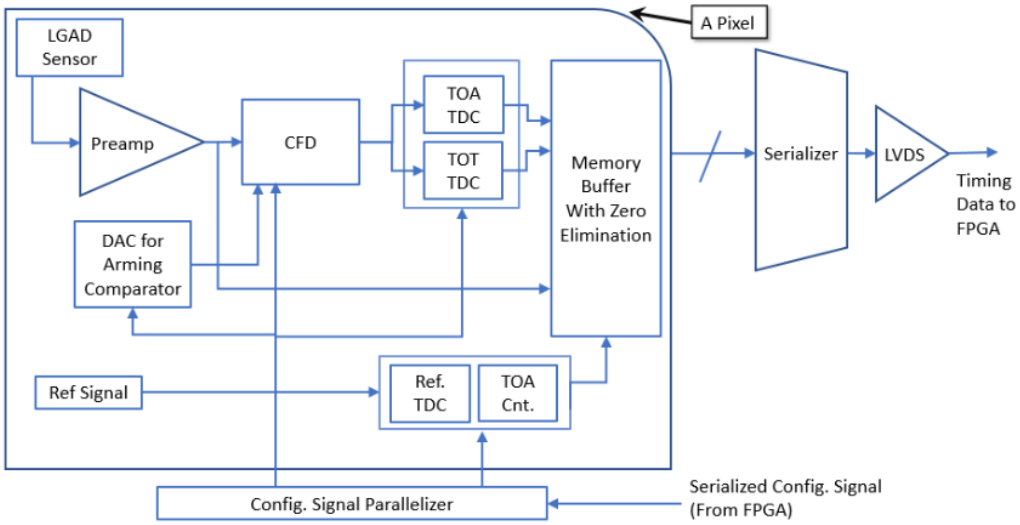

Figure 2. Schematic of the electronic readout to be implemented for every pixel.

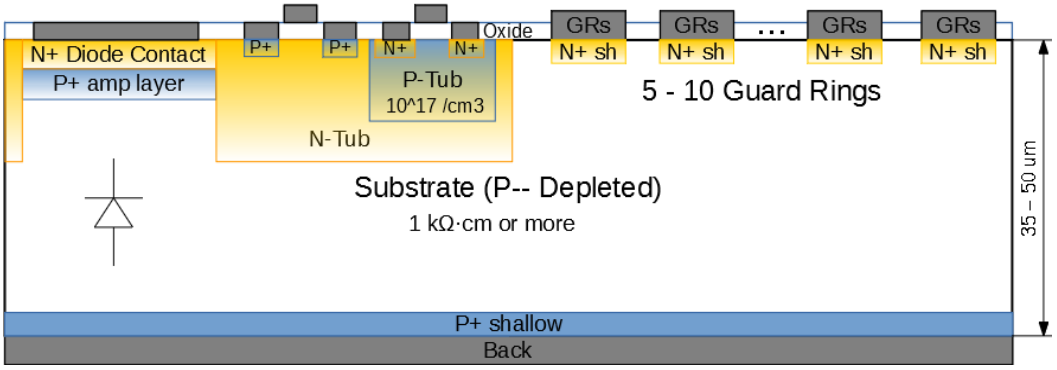

Figure 3. Design of the Argonne UFSD.

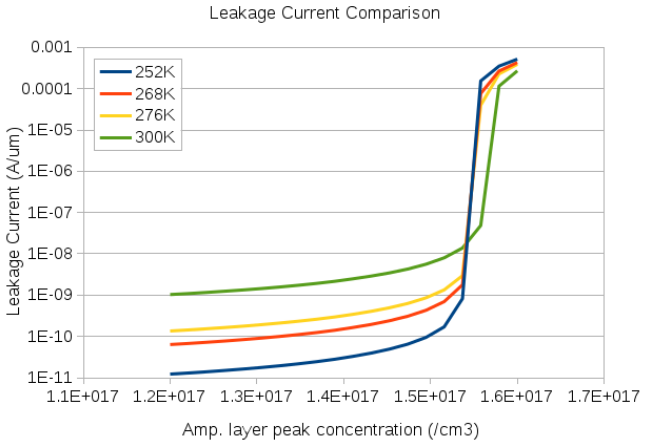

Figure 4. Leakage current as function of doping concentration for different operating temperatures.

d) Implementation of the 1st stage of the readout system

The first stages of the readout system are being prototyped with discreet components on a PCB board. The first stages include the shaper, amplifiers and the discriminators and have been fully simulated, see Fig. 5. Schematics of the circuitry and layout of the board are complete and the board is currently being fabricated.

e) Testing of sensors with the 1st stage of the readout system

Sensors will be tested with the prototype of the 1st stage of the readout system. These tests will include measurements with sources as well as data taking in the Fermilab test beam. At this stage, the TDC circuitry and logic is implemented through an FPGA toolkit, Ultra96, based on Xilinx Zynq UltraScale+ MPSoC.

f) **Implementation of the 1st stages of the readout system onto the sensor**

After careful testing of the prototype of the 1st stages of the readout system, its schematic will be implemented onto the sensor. This requires identification of a foundry, such as LFoundry, AMS, or Towerjazz, able to process LGAD sensors with implemented HVCMOS circuitry. As Argonne does not have the necessary EDA software licenses for the mask design and transistor level VLSI circuit simulation, this design work will be performed at Fermilab. Initial discussions about collaborating with Fermilab already took place with Gary Drake (senior engineer). Similar discussions took place with Ivan Peric from Heidelberg (AMS foundry CMOS design).

There are particular challenges to be faced when implementing the 1st stages of the electronic readout onto the sensor: identifying a foundry which is compatible with our integrated sensor design; the sensors being extremely thin (around 50 μm) and requiring processing on both sides without the use of a carrier wafer, with the risk of reducing the overall yield; the thickness of the sensor also requires extremely careful mechanical handling, as the wafer will be quite brittle; the doping concentration of the amplification layer is required to be very uniform imposing a particular challenge onto the fabrication process.

g) **Prototyping of sensors with the 1st stages of the readout system**

After the successful completion of the design of a sensor with implemented 1st stages of the readout system and after a thorough internal design review, the sensor will be prototyped in small quantities and undergo extensive testing. To reduce cost of the prototype fabrication, the production will be shared with other institutes in a multi-project wafer run.

h) Final design and prototyping steps (beyond the first year of funding)

The further steps in the development of integrated sensors include the implementation of the complete readout system, including the TDCs and the serializer (located on the rim of the sensor), on the HVCMOS device, and the subsequent prototyping and testing. In parallel to this work, we plan to develop a time distribution system with extremely low jitter. This work is planned to be performed in collaboration with institutes in Italy (Bologna and Torino).

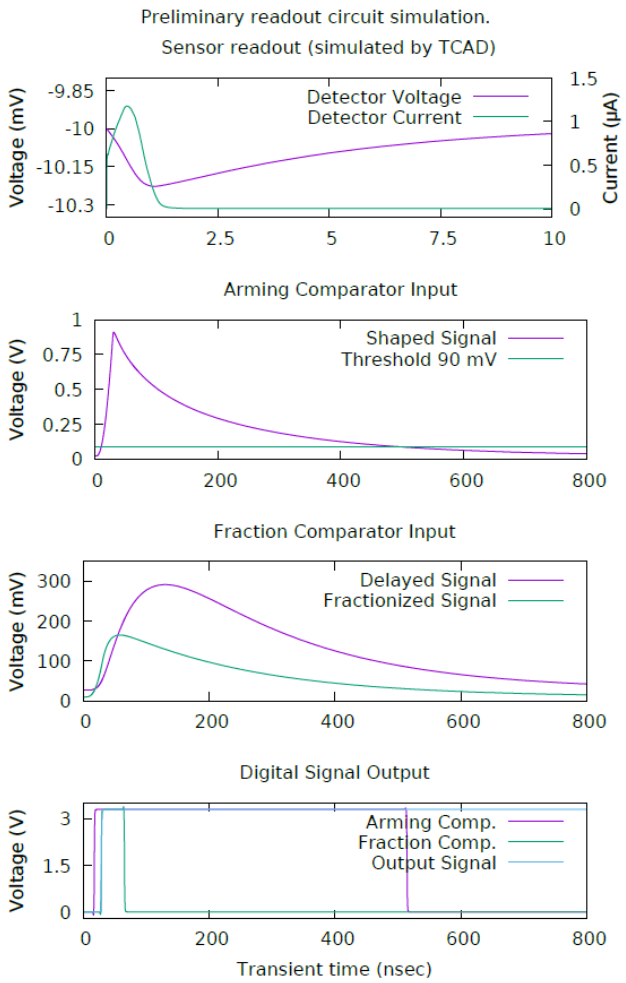

Figure 5. Simulation of the shaping, amplification and discriminator circuits.

Finally, sensors with a large channel count will be designed and produced for assembly in a small-scale prototype electromagnetic calorimeter, dubbed the PENTACAL. The latter will undergo tests in the Fermilab test beam.

Deliverables

The major deliverable of this proposal is a tested sensor with the 1st stages of the readout system implemented in HVCMOS. It will be used to

- Set performance benchmarks with the prototype
    - Time resolution
    - Jitter
    - Tracking efficiency
- Identify remaining technical challenges
- Identify potential vendors and cost for large scale applications

Funding request

We request support for postdoctoral research assistants in the amount of $125k (Manoj Jadhav 0.5 FTE and Taylor Shin 0.5 FTE, see below). The major task of the postdocs will be the implementation of the 1st stages of the electronic circuitry into the sensor. The proposed work will be carried out at Fermilab which possesses the necessary software tools. Funds are requested for the prototyping of the 1st iteration of the integrated sensor ($30k).

The postdoctoral research assistants will be supervised by José Repond and Jessica Metcalfe.

	Personnel funds	**Prototype fabrication**	**Sum**
Argonne National Laboratory	$125k	$30k	$155k

Table I. Summary of funding requests.

The Argonne team

We have assembled a competitive team to carry out the project:

José Repond: team leader
Leader in several past projects (ZEUS Barrel calorimeter construction, Small angle tracker for ZEUS, Digital Hadron Calorimeter). Experience with ASIC design (DCAL chip).

Jessica Metcalfe: silicon expert consultant
U.S. deputy project manager for the ITk pixel upgrade of ATLAS. L3 manager for the silicon pixel Modules for international ATLAS ITk pixel. 15 years of experience with silicon detectors.

Manoj Jadhav: postdoc working on silicon testing
Experience with the silicon fabrication and testing.

Taylor Shin: postdoctoral electronics engineer
Experience with the design of various silicon sensors, including for fast sensors for X-ray physics and the current Argonne LGAD sensor.

Argonne recently commissioned the Argonne Micro Assembly Facility (AMAF), a class 10,000 clean room with 4,200 square feet. The goal of the AMAF is to establish cooperation across the various divisions at Argonne with interest in silicon sensor development. Modules for the ATLAS upgrade inner tracker ITk will be assembled in this facility.

References

[1] J. Repond*, TOPSiDE: Concept of an EIC detector*, PoS DIS2018 (2018) 179.

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[3] M. A. Thomson, *Particle flow calorimetry and the PandoraPFA algorithm*, Nucl. Instr. Meth. **A611** (2009) 25-40.

[4] C. Adloff et al., *Hadronic energy resolution of a highly granular scintillator-steel hadron calorimeter using software compensation techniques*, JINST 7 (2012) P09017.

[5] H. F. W. Sadrozinski et al., *4D tracking with ultra-fast silicon detectors*, Rept. Prog. Phys. **81** (2018), no.2, 026101.

[6] H. F. W. Sadrozinski, *Measurement of timing precision of ultra-fast silicon detectors*, talk given at the Workshop on 'Picosecond timing detectors for physics and medical applications', Torino, Italy (2018).